University of California, Santa Barbara

Department of Electrical and Computer Engineering

Course Syllabus

ECE 125 *High Speed Digital Integrated Circuit Design* 4 units
(Elective)

Catalog Description:
Advanced digital VLSI design: CMOS scaling, nanoscale issues including variability, thermal management, interconnects, reliability; non-clocked, clocked and self-timed logic gates; clocked storage elements; high-speed components, PLLs and DLLs; clock and power distribution; memory systems; signaling and I/O design; low-power design.

Prerequisites:
ECE 124A or 137A with a minimum grade of C- in either.

Text, References, and Software:
Following books/references are used for different sub-topics:

1. *Digital Integrated Circuits: A Design Perspective* (2nd Edition), Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Prentice Hall, 2003.
2. *Fundamentals of Modern VLSI Devices*, Yuan Taur and Tak Ning, Cambridge Univ. Press., 1998.
3. *Design of High-Performance Microprocessor Circuits*, Chandrakasan, Bowhill, and Fox, IEEE Press, 2001.
4. *Selected Publications* provided on the course web site.

Topics Covered and Course Goals:

1. Basic and advanced issues in transistor level design of logic gates and components in various circuit styles (static CMOS, pseudo-NMOS, pass transistor, dynamic).

2. *Advanced issues in nanoscale MOSFETs:* short-channel effects, Latchup, leakage issues; alternate device architectures: SOI, double-gate (FinFETs) and Multi-gate FETs.

3. *Advanced IC processing technologies:* silicides, copper/low-k, metal-gate/high-k, shallow trench isolation, device engineering (halo doping, LDD, substrate orientation, strain etc) for improving I_on/I_off ratio and impact of process parameters on device and circuit level metrics.

4. *Advanced issues in nanoscale CMOS circuit designs:* interconnect (RLC delay) modeling, and optimization; power dissipation and thermal issues; variability and reliability.

5. Low-power vs high-performance design strategies, metrics for power-performance trade-offs (energy-delay product, power-delay product etc).

6. Design and analysis of i) high-speed components, DLLs and PLLs, ii) clock and power distribution networks, iii) I/O circuits iv) clocked and self-timed logic gates; clocked storage elements, v) memory systems including sense-amplifiers and other peripherals.

7. Circuit level analysis of emerging nanoelectronics: non-classical CMOS devices, 3-D ICs, carbon nanotube based devices and interconnects, nanowire FETs, and nano-electromechanical switches.

8. Become proficient in literature search, identifying new problems and defining individual research projects, technical (powerpoint) presentations and report writing (as per IEEE prescribed format).

Class/Laboratory Hours:
Lecture, 4 hours.

Contribution to Criterion 5
(b) One and one-half years of engineering topics, consisting of engineering sciences and engineering design appropriate to the student's field of study.

Contribution to Program Outcomes:

Course Goals	P1	P2	P3	P4	P5	P6
1		X				
2	X	X				
3		X				
4		X	X	X		
5		X	X	X		
6		X	X	X	X	
7		X	X	X	X	
8	X				X	

Prepared by: Kaustav Banerjee **Date: 03/21/2008**