

**CE Oral Screening Exam Problems: Spring 2005**  
**(ECE 15A and ECE 152A)**

Level 0:

1. What is the difference between a Mealy and Moore machine?
2. What is the fundamental difference between Verilog and C++?
3. What is the fundamental difference between a latch and a flip-flop? Why is this difference important in the design of sequential machines?

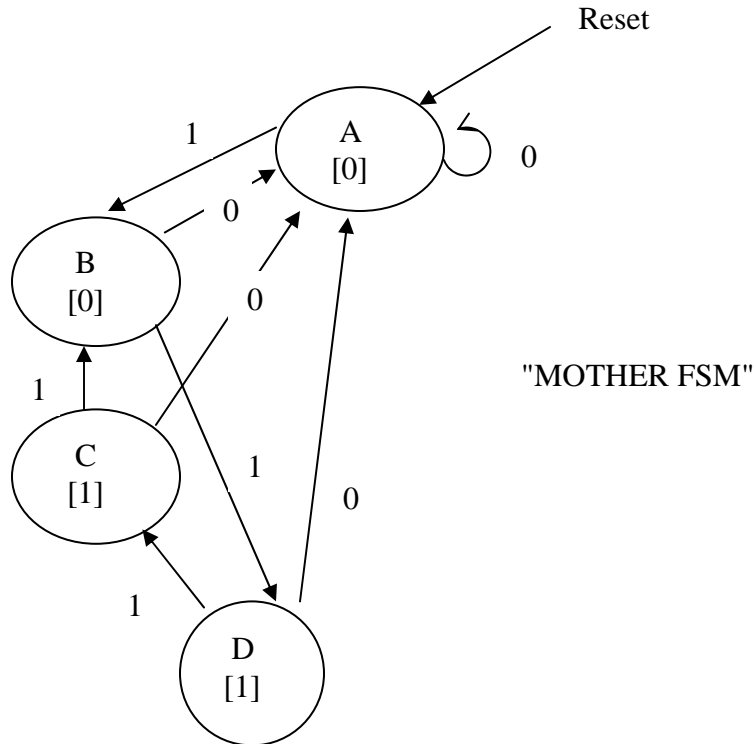
Level 1:

Design a finite state machine (FSM) that has a 1-bit data input X, a 1-bit synchronous control input called “Reset” and a 1-bit output Y, and operates as follows: The machine observes an incoming bitstream, **one bit at a time** (the observed bit is denoted by X). If Reset is asserted, the machine resets to the initial state (i.e. a state in which no bits have been observed thus far). If Reset is not asserted and the number of 1’s observed in the bitstream thus far is a multiple of 4, then the machine sets its output Y to 1; otherwise, the machine sets Y to 0.

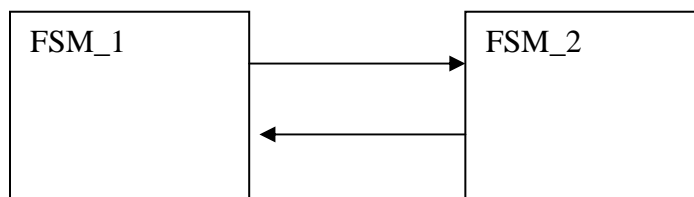
Draw the state diagram for this machine.

Level 2:

The state diagram of a FSM is given below:



We want to implement this FSM as two separate but interacting FSM's:



a) Design each of the interacting FSM's (i.e. show their state diagrams) and show precisely how they will interact.

b) What might be the advantage of implementing a large FSM as smaller interacting FSM's?